Claims

I claim:

1. A method of processing packets in a switch comprising:

selecting a first queue from at least three queues in a switch based on the cycle number (C) of a cycle;

flushing the first queue at the start of the cycle;

receiving at least one isochronous packet over a bus during the cycle;

placing the packet in a second queue based on the cycle number.

2. The method of claim 1 further comprising:

transmitting the packet from the second queue after two cycles.

3. The method of claim 1 wherein the first queue is chosen from four queues.

4. The method of claim 1 wherein the first queue is associated with a cycle that has a cycle number of C minus 1.

5. The method of claim 1 wherein the first queue is the same as the second queue.

6. The method of claim 1 wherein the first queue number is equal to the remainder of (C-1)/n wherein n is the number of queues in the switch.

7. The method of claim 1 wherein the second queue number is equal to the remainder of (C+2)/n wherein n is the number of queues in the switch.

8. The method of claim 1 further comprising:

transmitting packets in cycle C from a third queue wherein the queue number of the third queue is equal to the remainder of C/n wherein n is the number of queues in the switch.

9. The method of claim 1 further comprising:

setting a free pointer in the first queue to 0 at the end of the cycle; and

setting a used pointer in the first queue to 0.

10. The method of claim 1 further comprising:

setting a used pointer in the second queue to 0 at the end of the cycle; and

setting a free pointer in the second queue to n.

11. A system of processing packets in a bus switch comprising:

means for storing data in queues;

means for selecting appropriate queuing means for each set of incoming data;

means for directing the set of incoming data to the appropriate queuing means; and

means for flushing data from the queuing means.

12. The system of claim 11 further comprising means for receiving the incoming data and wherein the incoming data includes isochronous packets.

13. A switch in a network comprising:

a buffer memory including at least three egress queues; and

a processor configured to direct incoming isochronous packets into one of the egress queues based on a cycle number of the switch and configured flush another of the egress queues based on the cycle number.

14. The switch of claim 13 wherein the switch is configured to be used with at least one bus.

15. The switch of claim 13 wherein the switch is configured to be used with a connection selected from the group: ethernet bus, asynchronous transfer mode bus, and IEEE 1394 standard bus.

16. The switch of claim 13 further comprising:

at least one ingress port; and

at least one egress port

wherein each egress port is associated with at least three egress queues.

17. The switch of claim 16 wherein the egress queues store data to be transmitted by the processor from each egress port.

18. The switch of claim 13 wherein the buffer memory includes four queues.

19. The switch of claim 13 wherein the processor is configured to direct the incoming isochronous packets into the egress queue number equal to the remainder of (C + 2)/n wherein n is the number of queues in the switch.

20. The switch of claim 13 wherein the processor is configured to flush the egress queue number equal to the remainder of (C - 1)/n wherein n is the number of queues in the switch.

21. The switch of claim 13 wherein the processor is configured to transmit the isochronous packets from the egress queue number equal to the remainder of C/n wherein n is the number of queues in the switch.